

Logic Gates

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Every logic gate has one or more inputs and exactly one output, and can be described four equivalent ways: **logic symbol**, **truth table**, **Boolean expression**, **timing diagram** (see timing-diagrams¹ for the last of these, and for real-gate propagation delay / rise / fall times).

The 7 basic gate types

Gate	Behaviour	Truth table ($A, B \rightarrow X$)
NOT (inverter)	Inverts the input	$0 \rightarrow 1, 1 \rightarrow 0$
AND	$X = 1$ iff all inputs are 1	$00 \rightarrow 0, 01 \rightarrow 0, 10 \rightarrow 0, 11 \rightarrow 1$
OR	$X = 1$ iff at least one input is 1	$00 \rightarrow 0, 01 \rightarrow 1, 10 \rightarrow 1, 11 \rightarrow 1$
NAND	$X = 1$ iff at least one input is 0 (NOT AND)	$00 \rightarrow 1, 01 \rightarrow 1, 10 \rightarrow 1, 11 \rightarrow 0$
NOR	$X = 1$ iff all inputs are 0 (NOT OR)	$00 \rightarrow 1, 01 \rightarrow 0, 10 \rightarrow 0, 11 \rightarrow 0$
XOR	$X = 1$ iff exactly one input is 1 (“odd function”)	$00 \rightarrow 0, 01 \rightarrow 1, 10 \rightarrow 1, 11 \rightarrow 0$
XNOR	$X = 1$ iff inputs are the same (“even function”)	$00 \rightarrow 1, 01 \rightarrow 0, 10 \rightarrow 0, 11 \rightarrow 1$

Useful to remember: **XOR is the odd function**, **XNOR is the even function** — this generalises directly to more than 2 inputs ($XOR = 1$ iff an odd number of inputs are 1).

¹[courses/csse2010/timing-diagrams.pdf](#)

Universal (complete) gates

All circuits can be constructed from **NAND-only** or **NOR-only** gates — these are called **complete** (or universal) gates, because NOT, AND, and OR can each be built purely from one gate type:

- **NOT**: a NAND (or NOR) gate with both inputs tied together.
- **AND**: two NANDs in series (NAND followed by another NAND used as an inverter), or the NOR equivalent.
- **OR**: built similarly from NAND-only or NOR-only combinations.

NAND and NOR are preferred in practice because they're easier to build from transistors than AND/OR directly.

Gates on ICs

Example: the **74HCT00** integrated circuit packages four independent 2-input NAND gates into a single 14-pin DIP chip (V_{cc} = power e.g. 5V, GND = ground/0V; pin spacing 0.1"×0.3", chip ~15mm long).