CSSE2010/CSSE7201 — Introduction to Computer Systems

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Staff

- **Dr Martin Ploschner** — course coordinator & lecturer
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- Email (both coordinators): csse2010@eecs.uq.edu.au
- Office hours: listed on Blackboard
- A large group of tutors support the Learning Lab sessions

Textbook

No textbook required — some references are listed in the course profile.

Study formula

1L-2P-1L-2P-3S-1E per week (L = Lecture, P = Practical, S = Self study, E = Exercise/Problem solving).

Course structure

The course builds up through the levels of computer abstraction (see binary-number-representations[1] and logic-gates[2] for the Level 0 material covered first):

- **Weeks 1-5ish** — Hardware (digital logic, gates, AVR microcontroller hardware)
- **Weeks 6-8ish** — Low-level software (assembly language)
- **Weeks 9-13ish** — High-level software

(Boundaries are approximate — based on the "levels of abstraction" overview diagram shown in Lecture 1, not an exact week-by-week breakdown.)

Course learning activities

- In-person mode only.
- **Lectures**: Mon 2pm AEST and Thu 8am AEST.
- **Learning Labs** (practical sessions): in-person at 47-104, two sessions per week.
  - Sign up for a *pair* of lab sessions — [PRA-x-P2, PRA-x-P1] — 7 pairs to choose from.
  - PRA-x-P2 sessions run Mon-Tue; PRA-x-P1 sessions run Thu-Fri.
  - **No P2 sessions in week 1** (Mon-Tue) — week 1 labs start from Thursday (P1 sessions only).
  - From week 2 onward, both P2 and P1 sessions run every week.
  - Sign-on issues: contact eait.mytimetable@uq.edu.au.
- A lab kit is loaned in weeks 3-4 and must be returned by the end of the course (or within 3 business days of dropping the course, to the EECS school office at 78-425).
- Practice exercises and weekly quizzes are provided but **not assessed**.

Assessment

Component	Weight	Due	Notes
In-semester exam	20%	In-semester Saturday, 5/09/2026 – 20/09/2026	Personal exam timetable emailed
Lab exam (Digital Logic Design)	10%	Week 7	In-person

[1] courses/csse2010/binary-number-representations.pdf
[2] courses/csse2010/logic-gates.pdf

Component	Weight	Due	Notes
AVR Programming Assignment	20% (CSSE2010) / 5% + 15% (CSSE7201)	23/10/2026, 4:00pm	**Hurdle**
AVR Programming Assignment (Demo)	Pass/Fail	Week 13	**Hurdle**
Final Examination	50%	End of semester exam period, 7/11/2026 – 21/11/2026	**Hurdle**

- **CSSE2010**'s AVR Programming Assignment is Practical-only (20%).
- **CSSE7201**'s AVR Programming Assignment splits into a Theoretical Part 1 (5%) and Practical Part 2 (15%).
- All exams/assessments are in-person with identity verification.

Resources

- Course Blackboard site: announcements, readings, notes, software downloads.
- Discussion Board (Edstem) for technical questions.
- Admin or content questions: use consultation hours, or email csse2010@eecs.uq.edu.au to book an appointment.

Lectures

- 2026-07-27-course-intro-bits-bytes-binary[3]
- 2026-07-30-intro-to-logic-gates[4]
- 2026-08-04-binary-arithmetic[5]

Exercises

- week-one-exercises[6]
- week2-lab-majority-function-circuit-design[7]

[3] courses/csse2010/2026-07-27-course-intro-bits-bytes-binary.pdf
[4] courses/csse2010/2026-07-30-intro-to-logic-gates.pdf
[5] courses/csse2010/2026-08-04-binary-arithmetic.pdf
[6] courses/csse2010/week-one-exercises.pdf
[7] courses/csse2010/week2-lab-majority-function-circuit-design.pdf