

Circuit Schematics

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A **logic diagram** shows the *idea* of a circuit and is hardware-independent (see logic-gates¹). A **circuit schematic** goes further: it tells you how to actually **build** the circuit on real hardware — labelled ICs, pin numbers, power connections — so it's hardware-specific. Schematics are drawn for practicals and assessment using 74-series logic chips and the CSSE2010/CSSE7201 IO Board (see device-pinouts² for pin layouts).

Source: *CSSE2010/CSSE7201 - Guide to Drawing Circuit Schematics* (Blackboard, v2.3). The rules below are that document's requirements; the errors are its annotated bad-schematic example.

Required elements

Every circuit schematic must show:

- **Labelled inputs and outputs** — every input/output needs a sensible, unique name. Inputs and outputs use different arrow symbols (which way they point), and by convention inputs are drawn on the left, outputs on the right.
- **Labelled devices** — each physical device (chip or IO board) gets a unique identifier: one or more letters for the device type, then a sequential number starting from 1.
 - Logic chips: U1, U2, U3, ...
 - IO board: I01 (I02 for a second board, etc.) — when a group of inputs/outputs all belong to the same IO board, it only needs to be labelled once for the whole group, not per signal.

¹[courses/csse2010/logic-gates.pdf](#)

²[courses/csse2010/device-pinouts.pdf](#)

- **Gate labels within a chip** — where a chip contains multiple gates, each gate is labelled A, B, C, ... after the chip ID, separated by a colon (e.g. U1:A, U1:B). Labels can be assigned to gates in any order. A chip with only one gate/device doesn't need a gate letter (just U3).
- **Device type** — written on the line below the device ID (e.g. 74HCT00, 74HCT04, IOBOARD).
- **Pin numbers** — every pin used must be numbered per the actual device pinout (see device-pinouts³).
- **Power supply connections** — shown once per device *type*, not per individual chip. Where two+ chip types share the same power pins, they can be grouped together. The IO board doesn't need power connections shown.

Common errors

From the guide's worked example of a bad schematic:

1. **Duplicate names** — two inputs given the same name (e.g. both called A). Every input needs a unique name.
2. **Missing junction dots** — where wires join or split, a dot must mark the connection. Wires that merely cross on the page, with no dot, are *not* electrically connected.
3. **Gate label exceeds chip capacity** — e.g. labelling a gate U1:E on a 74HCT00, which only has four 2-input NAND gates (A–D). A fifth gate needs a new chip ID (U2:A).
4. **Wrong device for the gate type** — a different gate type (e.g. NOT vs NAND) needs its own chip identifier; you can't add it under an existing chip's ID.
5. **Reusing pin numbers** — e.g. U1:C using the same pins as U1:A. You can't use the same physical gate twice.
6. **Inconsistent device type** — every gate labelled U1:something must show the *same* chip type; a chip ID can't switch part-way through (e.g. U1:D shown as a 74HCT47 when the rest of U1 is a 74HCT00).
7. **Output errors** — two distinct mistakes to watch for:
 - a. Using the input-arrow symbol where an output-arrow symbol is needed.
 - b. Wiring a gate output directly into another output pin/signal — an input should never be tied straight to a gate's output; gate outputs should only feed output devices (e.g. LEDs) or the inputs of other gates. Doing this may destroy the device.

³courses/csse2010/device-pinouts.pdf